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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/888,096 | 06/22/2001 | Lauren B. Wenzl | X-662 US | 7929 |

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| EXAMINER | |
|---|---|
| ZHEN, LI B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2126 | |

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/888,096 | WENZL, LAUREN B. | |
| | Examiner | Art Unit | |
| | Li B. Zhen | 2126 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 – 11 are pending in the application.

### *Response to Arguments*

2. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1 – 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent NO. 6,477,611 to Chang.**

5. As to claim 1, Chang teaches an interface [CAP interface circuit 30, Fig. 1; col. 4, lines 62 – 67] for an electronic device [computer 11, Fig. 1; col. 4, lines 47 – 61] being coupled to a peripheral device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32], the interface including:

a configurable hardware interface [CAP interface circuit 30, Fig. 1; col. 4, line 62 – col. 5, line 17], wherein the configurable hardware interface includes:

a programmable logic device (PLD) [FPGA 31, Fig. 1; col. 5, lines 3 – 17];

a memory coupled to the PLD [FPGA configuration buffer 32, Fig. 1; col. 4, lines 62 – 67];

a control interface for controlling the PLD and the memory [CAP interface circuit 30; col. 4, line 62 – col. 5, line 18]; and

a communication interface [FPGA 31 is electrically connected to CAP I/O bus 15 through a connector 34; col. 4, line 62 – col. 5, line 2] for receiving information from the peripheral device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32] and enabling the control interface [at least one conductor of CAP I/O Bus 15, which may be called IN_CAP conductor (or line or pin) 17, is used to communicate the identification number for module 12 from module 12 to computer 11, Fig. 1; col. 5, lines 30 – 43]; and

a storage component [computer memory 33, Fig. 1; col. 6] for storing a bitstream that configures the configurable hardware interface to implement a driver of the external device [CAP Bus computer memory 33 includes three databases...FIG. 2. A first database, referred to as Domain "A" CAP Bus Database 51, has i entries each having a bus logic FPGA image file 52 and a device driver 53. A second database, referred to as

Protocol Bus Database 55, has j entries each having a bus logic FPGA image file 56 and a protocol driver 57; col. 6, lines 21 – 46].

6. As to claim 2, Chang teaches the storage component includes volatile memory [computer memory 33, Fig. 1; col. 6 and col. 4, lines 47 – 52].

7. As to claim 3, Chang teaches the storage component includes static random access memory [computer memory 33, Fig. 1; col. 6 and col. 4, lines 47 – 52].

8. As to claim 4, Chang teaches the communication interface includes one of a universal serial bus, a parallel port connector, a serial port connector [CAP I/O bus 15 through a connector 34; col. 5, lines 1 – 2], and a small computer system interface (SCSI).

9. As to claim 5, Chang teaches the communication interface establishes synchronous communication between the electronic device and the peripheral device [establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 15 – 30].

10. As to claim 6, Chang teaches the memory includes at least one lookup table [CAP Bus computer memory 33 includes three databases; col. 6, lines 23 – 46].

11. As to claim 7, Chang teaches including at least one of an Ethernet interface, a modem interface, and a custom interface for communicating with the peripheral device [Any conventional communication device compatible with standard protocol port 24, such as an analog modem 27, may be electrically connected with connector 23 to allow communication with external computers and networks such as a server 28 accessible through the Internet; col. 4, lines 52 – 61].

12. As to claim 8, Chang teaches a method of facilitating communication between two devices [establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 15 – 30], the method comprising:

identifying a host device [computer 11, Fig. 1; col. 4, lines 47 – 61], from the two devices, that controls communication between the two devices [the device driver is executed, thereby establishing communication operation between computer 11 and module 12; col. 7, lines 39 – 54];

identifying a peripheral device that accepts commands from the host device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32];

storing a plurality of bitstreams in the host device, the plurality of bitstreams corresponding to drivers [CAP Bus computer memory 33 includes three databases...FIG. 2. A first database, referred to as Domain "A" CAP Bus Database 51, has i entries each having a bus logic FPGA image file 52 and a device driver 53. A

second database, referred to as Protocol Bus Database 55, has j entries each having a bus logic FPGA image file 56 and a protocol driver 57; col. 6, lines 21 – 46]; and

determining whether one of the drivers is a driver of the peripheral device [If the configuration information for module 12 is not located in Domain "A" (block 75), col. 7, lines 55 – 67; If the configuration information for module 12 is not located in Domain "A" or Domain "B" as determined in block 87, col. 8, lines 6 – 8],

wherein if on of the drivers is the driver of the peripheral device, then selecting that bitstream corresponding to the driver of the peripheral device [block 77 the corresponding CAP Bus logic FPGA image file, and device driver for ID.sub.x are retrieved from CAP Bus computer memory 33 and loaded into FPGA configuration buffer 32; col. 7, lines 39 – 54],

otherwise, directing the host device to receive a bitstream from the peripheral device [configuration information is retrieved from the location corresponding to the identification number from one of a plurality of locations including the first device, the second device and an external source; col. 3, lines 54 – 63]; and

configuring a programmable logic device (PLD) [FPGA 31, Fig. 1; col. 5, lines 3 – 17] in the host device with the bitstream to implement the driver of the peripheral device [FPGA 31 then configures the CAP Bus in accordance with the contents of FPGA configuration buffer 32, as described in block 79, and, in block 80, the device driver is executed, thereby establishing communication operation between computer 11 and module 12; col. 7, lines 39 – 54].

13. As to claim 9, Chang teaches storing a plurality of designations [locations] in the PLD, wherein each designation corresponds to one of the plurality of bitstreams [configuration information necessary to configure FPGA 31 to interface correctly with module 12 is available in one of four locations: onboard computer 11 in CAP Bus memory 33 (which shall be referred to as Domain "A"); onboard module 12 in CAP module memory 42 (which shall be referred to as Domain "B"); col. 5, line 65 – col. 6, line 13], wherein determining includes searching the plurality of designations [block 75 and block 87, Fig. 5A; col. 8, lines 6 – 8].

14. As to claim 10, this is rejected for the same reasons as claim 6 above.

15. As to claim 11, Chang teaches each designation includes an addresses for one of the plurality of bitstreams stored in the host device [CAP I/O Bus specification to find the entry in CAP Bus ID directory 60 whose secondary memory pointer corresponds to the bus logic FPGA image files, device driver, and/or protocol driver needed for module 12; col. 6, lines 56 – 65], and wherein selecting includes accessing an address in the host device for the bitstream to implement the driver of the peripheral device [retrieving that information from the location specified by the identification, reconfiguring the I/O Bus of computer 11 to be compatible with the I/O Bus configuration of external module 12, and establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 16 – 30].

***Conclusion***

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2126

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